Amendments to the Claims

Please cancel Claims 1-4. Please add new Claims 5-25. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1-4. (canceled)

5. (new) A semiconductor memory comprising:

plural arrays of storage cells;

at least one secondary databus, centrally located between the plural arrays, extending in a first direction; and

a plurality of primary databuses coupled to the at least one secondary databus, each of the plurality of primary databuses coupled to one of the plural arrays and the primary databuses extending in a second direction orthogonal to the first direction.

6. (new) The semiconductor memory of claim 5 wherein:

each primary databus is coupled to a plurality of lines of bit line sense amplifiers with each primary databus coupled to at least one bit line sense amplifier in each line of sense amplifiers, and

each bit line sense amplifier is coupled to a bit line pair, the bit line pairs being parallel to the primary databuses.

7. (new) The semiconductor memory of claim 6 wherein the bit lines sense amplifiers fully sense bit line data to full logic levels.

8. (new) The semiconductor memory of claim 5 wherein the arrays are DRAM arrays.

9. (new) The semiconductor memory of claim 5 wherein the arrays are mirror images of each other.

10. (new) The semiconductor memory of claim 5 further comprising databus sense amplifiers coupled between the primary and secondary databuses.

11. (new) The semiconductor memory of claim 10 wherein said databus sense amplifiers are selectively coupled to the at least one secondary databus through isolation devices.

12. (new) The semiconductor memory of claim 10 wherein each databus sense amplifier is selectively coupled to a plurality of said primary databuses.

13. (new) The semiconductor memory of claim 5, comprising an application specific memory.

14. (new) The semiconductor memory of claim 5, comprising an embedded memory in an application specific integrated circuit.

15. (new) The semiconductor memory of claim 5 wherein the at least one secondary databus is a single databus time shared by arrays on both sides thereof.

16. (new) The semiconductor memory of claim 5 wherein the at least one secondary databus comprises two parallel secondary databuses.

17. (new) A memory comprising:

plural memory arrays, each array comprising:

pairs of bit lines, each pair being coupled to a corresponding bit line sense amplifier;

word lines crossing the bit line pairs; and

storage cells coupled to the bit lines, each having an enable input coupled to a word line;

pairs of primary databuses parallel to the bit lines, coupled to a plurality of bit line sense amplifiers through first access devices; and

pairs of secondary databuses orthogonal to the primary databuses, centrally located between the plural arrays.

18. (new) The memory of claim 17 wherein the bit line sense amplifiers are arranged in plural lines and each primary databus pair is selectively coupled to at least one bit line sense amplifier in each line of sense amplifiers

19. (new) The memory of claim 17 wherein the storage cells are charge storage cells.

20. (new) The memory of claim 17 wherein each of two arrays is a mirror image of the other.

21. (new) The semiconductor memory of claim 17, comprising an application specific memory.

22. (new) The semiconductor memory of claim 17, comprising an embedded memory in an application specific integrated circuit.

23. (new) A method of accessing memory comprising:

selectively enabling charge storage cells in at least one of plural arrays of charge storage cells, the charge storage cells connected to bit line pairs using word lines crossing the bit line pairs;

sensing stored charge for enabled charge storage cells by bit line sense amplifiers;

selectively coupling the bit line sense amplifiers to pairs of primary databuses through first access transistors, the primary databus pairs being parallel to the bit line pairs; and

selectively coupling the primary databus pairs to secondary databus pairs through second access transistors, the secondary databus pairs being orthogonal to the primary databus pairs and centrally located between the plural arrays.

24. (new) The method of claim 23 further comprising:

in a read operation, selectively coupling each pair of primary databuses to plural databus sense amplifiers through respective isolation transistors

25. (new) The method of claim 23 wherein the bit lines sense amplifiers fully sense bit line data to full logic levels.